Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 – 17. (cancelled)

Claim 18. (currently amended) A circuit comprising:

at least one global supply;

M voltage sources, wherein M is an integer number greater than two (2); ~~and~~

a switching network having M terminals, wherein each terminal is coupled to an output from one of the M voltage sources[[,]] ;

the switching network containing N switch structure circuitries to electrically couple the at least one global supply to the M terminals, wherein N is an integer of at least two (2);

each of the N switch structure circuitries containing a first and a second switch to couple the at least one global supply to a first and a second of the M terminals, respectively; and

each of the N switch structure ~~circuitry~~ circuitries further containing a third switch to electrically ~~couple~~ connect pairs of the outputs of the M voltage sources, wherein the ~~coupling~~ connection of pairs of the outputs is based on a mapping selected from the group consisting of connecting pairs of all of the outputs together, connecting at least two of the outputs together, predeterminately connecting at least two of the outputs together, and dynamically determinately connecting at least two of the outputs together.

Claim 19. (original) The circuit of claim 18, wherein some of the voltage sources produce outputs with the same voltage potential.

Claim 20. (original) The circuit of claim 19, wherein the outputs of voltage sources coupled together all have the same voltage potential.

Claim 21. (currently amended) The circuit of claim 19, ~~wherein switches couple the outputs, and~~ wherein outputs of voltage sources with different voltage potentials are not connected by switches.

Claim 22. (original) The circuit of claim 18, wherein the mapping is stored in a memory.

Claim 23. (original) The circuit of claim 18, wherein the mapping is dynamically computed.

Claim 24. (currently amended) The circuit of claim 18, ~~wherein switches couple the outputs, and~~ wherein the mapping specifies the state of each switch in the switching network.

Claim 25. (cancelled)

Claim 26. (original) The circuit of claim 18, wherein each output is connected to two other outputs via a switch.

Claim 27. (original) The circuit of claim 26, wherein the outputs are connected in a circular fashion.

Claim 28. (original) The circuit of claim 18, wherein the M voltage sources supply power to M power domains.

Claim 29. (original) The circuit of claim 18, wherein the M voltage sources supply power to M power sub-domains within a single power domain.

Claim 30. (cancelled)

Claim 31. (currently amended) The circuit of claim ~~30~~ 18, wherein the switches are each ~~switching structure is~~ a transistor[[,]] ~~the~~; wherein a first terminal is the transistor's source, ~~the~~ a second terminal is the transistor's drain, and ~~the~~ a control signal line is coupled to the transistor's gate.

Claim 32. (currently amended) An integrated circuit comprising:

a circuitry block; and

a plurality of power supplies, each coupled to the circuitry block, each power supply comprising:

M voltage sources, wherein M is an integer number greater than one (1); ~~and~~

a switching network having M terminals, wherein each terminal is coupled to an output from one of the M voltage sources, the switching network containing switch circuitry to electrically ~~couple~~ connect pairs of the outputs of the M voltage sources, and the switching network further containing a voltage switch between each of the M voltage sources and a selected power supply~~, wherein the coupling of the outputs is based on a mapping~~.

Claim 33. (original) The integrated circuit of claim 32, wherein the circuitry block comprises a plurality of circuit blocks, and wherein there is at least one power supply associated with each circuit block.

Claim 34. (original) The integrated circuit of claim 33, wherein all power supplies are identical.

Claim 35. (original) The integrated circuit of claim 33, wherein each power supply may be designed differently.

Claim 36. (original) The integrated circuit of claim 33, wherein each circuit block and its associated power supply are located adjacent to one another on the integrated circuit.

Claim 37. (new) A circuit comprising:

at least two power domains;

at least two voltage sources;

a switching structure having a first switch coupled between a first of the at least two voltage sources and a first of the of the at least two power domains, and a second switch coupled between one of the at least two voltage sources and a second of the at least two power domains, and a third switch connected between two of the at least two power domains; and

the first, second and third switches operable to activate electrical coupling based on values of a first, second and third control signal line.

Claim 38. (new) The circuit of Claim 37, wherein the third control signal line is logically derived from the first and second control signal lines.

Claim 39. (new) The circuit of Claim 37, wherein the first, second and third switches each comprise a MOSFET (metal oxide semiconductor field effect transistor), a first, second and third MOSFET, respectively.

Claim 40. (new) The circuit of Claim 39, wherein the MOSFETs have thick oxide to provide low-leakage characteristics.

Claim 41. (new) The circuit of Claim 39, wherein the width of the first and second MOSFETs are approximately equal and the width of the third MOSFET between the at least two power domains is on the order of 10 to 20 percent the width of the first and second MOSFETs.

Claim 42. (new) The circuit of Claim 37, wherein the first, second and third switches each comprise a P–type MOSFET (metal oxide semiconductor field effect transistor).

Claim 43. (new) The circuit of Claim 37, wherein the second switch is coupled between the first of the at least two voltage sources and a second of the at least two power domains.

Claim 44. (new) The circuit of Claim 43, wherein the first, second and third switches each comprise a P–type MOSFET (metal oxide semiconductor field effect transistor).